REMARKS

Claims 10 and 21-40 are pending in the Application.

Claims 10 and 21-40 stand rejected.

I. REJECTION UNDER 35 U.S.C. § 103

Claims 10 and 30 have been rejected under 35 U.S.C. § 103 as being unpatentable over *Patt, et al.*, "Alternative Implementations of Hybrid Branch Predictors," Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257 ("*Patt*") in view of *Talcott et al.*, U.S. Patent No. 6,289,441 ("*Talcott*") in further view of *Shimomura et al.*, U.S. Patent No. 5,737,381 ("*Shimomura*"). The Applicants respectfully traverse the rejection of claims 10 and 30 under 35 U.S.C. § 103.

Claim 10 is directed to a processing system including a first branch history table comprising a plurality of bimodal accessed entries for storing a first set of branch prediction bits, a second branch history table comprising a plurality of fetch-based accessed entries for storing a second set of branch prediction bits, a selector for selecting in response to a selection control bit selected from a set of selection control bits, a bit from a selected one of the sets of bits accessed from the first and second branch history tables, and a selector table comprising a plurality of entries for storing the set of selector bits as a function of a performance history of the first and second sets of branch prediction bits stored in the first and second branch history tables, wherein each the entry in the tables comprises a one-bit counter.

Patt allegedly teaches all of the limitations of claim 10 but for the one-bit counters and the fetch-based accessed branch history table. (Paper No. 11, page 3.) The Examiner relies on *Talcott* as teaching the fetch-based branch history accessed table entries. (*Id.*) The Examiner further admits that neither *Patt* and *Talcott* teach one-bit counters. (*Id.*) The Applicant will address these allegations in turn.

To cure the admitted defect in *Patt*, the Examiner first engrafts the branch predictor of *Talcott* into *Patt*. (Paper No. 11, page 3.) The Examiner asserts that it would be obvious to

implement the branch prediction scheme of *Patt* using the fetch bundle prediction of *Talcott* "to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs." (Paper No. 11, page 3.) There is no evidence that the Examiner has found this motivation in one of the possible sources thereof. *See* MPEP § 2143.01. This is just the type of broad conclusory assertion regarding the teachings of the references that has been deemed to fail to provide a motivation or suggestion for combining references necessary for a *prima facie* showing of obviousness. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1616-17 (Fed. Cir. 1999) (stating that the best defense against the powerful attraction of hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references). Plainly, if such a motivation were adequate, the requirement would become a nugatory because it could always be the that the modification or combination was made to improve speed, efficiency, etc. It is a rare circumstance that a combination or modification would be made to increase cost, use more energy, slow something down, or some other such rationale. Furthermore, to the extent the Examiner is relying on objective evidence at all, it is evidence gleaned solely from the Application. (*See e.g.* Background Information, page 3, lines 7-10.) A showing of obviousness cannot be predicated on knowledge gleaned only from the Application. *In re McLaughlin*, 443 F.2d 1392, 1395, 170 U.S.P.Q. 209, 212 (C.C.P.A. 1971) (stating that a reconstruction must not rely on knowledge gleaned only from the applicant's disclosure).

Neither has the Examiner provided any evidence of a reasonable expectation of success in modifying *Patt* to make the claimed invention. Such a showing is also required to make a *prima facie* showing of obviousness. MPEP § 2143. The reasonable expectation of success must be found in the prior art, not the Application. *Id.* The Examiner is using the Application as a template to reconstruct the invention from parts harvested from the references, and thus, any expectation of success is derived solely from the Application.

With respect to the one-bit counters, the Examiner asserts that a two-bit counter "naturally comprises" a one-bit counter, and that *Shimomura* is evidence that it was known at the

time of the invention to implement one-bit counters. (Paper No. 11. page 3.) The Applicant respectfully disagrees that a two-bit counter comprises a one-bit counter.[1] The Applicant has previously addressed this assertion in detail. (*See e.g.* Applicant's Second Rely Under 37 C.F.R. § 1.111, mailed September 5, 2003, (hereinafter, the "Applicant's Second Reply," page 5.) A two-bit counter has two output bits that are correlated. A one-bit counter has a single output bit, and two one-bit counters have two single output bits, that is the output bits are uncorrelated. The Examiner's assertion is tantamount to stating that the value "10" comprises the value "1" or, equivalently, the value "0," which is contrary to common knowledge. Contrary to PTO practice, the Examiner has yet to address the substance of the Applicant's showings. *See* MPEP § 707.07(f). This is not to say that a two-bit counter cannot be fabricated from one-bit counters and the appropriate interconnections. However, it would be appreciated by persons of ordinary skill in the art that the result is an integral device that is different than two one-bit counters, which have a different truth table than the two-bit counter. Thus, it is immaterial that *Shimomura* discloses a one-bit counter.

Moreover, as the Applicant has previously shown, *Patt* cannot be modified to make the invention of claim 10. *Patt* teaches, in particular, a Branch Predictor Selection Table (BPST) having two-bit counters. (*Patt*, Section 2, page 252; *see also* Applicant's Second Reply, page 5.) The teaching in *Patt* with respect to such a BPST discloses hybrid branch prediction schemes in which the counters in the BPST keep track of the currently more accurate predictor for a branch. (*Id.*) The two-level prediction scheme disclosed in *Patt* is a combination of the hybrid scheme with a first level history based on branch history registers (BHRs). (*Patt*, Section 4.1, page 255; *see also* Applicant's Second Reply, page 5.) *Patt* explicitly teaches that the BPST used in the two-level prediction scheme is a table of two-bit counters just as disclosed in conjunction with the hybrid prediction scheme (*Patt*, Section 4.2, pages 255-56.) As discussed in conjunction therewith, as noted hereinabove, the two-bit counters of the BPST keep track of the predictor which is currently more accurate for a particular branch. This is an essential element of the two-

1 As the Applicant previously noted, this statement is similar to asserting that a bicycle "comprises" a unicycle. A bicycle is not a unicycle nor does a bicycle "teach" a unicycle because it has two wheels and a unicycle has one.

level prediction scheme of *Patt*; it provides the second level of history. (*See Patt*, Section 4.1, page 255.)

A *prima facie* showing of obviousness requires, *inter alia*, that there must be a reasonable expectation of success in modifying or combining the references to make the claimed invention. MPEP § 2143. Furthermore, the reasonable expectation of success must be found in the references prior art, not the Applicant's disclosure. *Id.* The Examiner has provided no evidence whatsoever of a reasonable expectation of success.

Neither is it sufficient to assert that a person of ordinary skill in the art would have been motivated to modify *Patt* to incorporate one-bit counters because it would have been less hardware space and thus money, or a simple design structure. (Paper No. 11, page 4.) Even if, for the sake of argument, it is assumed that the incorporation of one-bit counters leads to less cost or a simpler design structure, the Applicant respectfully submits that both *Patt* and *Talcott* would be aware of such "motivations" and, thus, there may be considerations that outweigh any such advantage.[2] For example, two-bit counters may be more tolerant of a branch going in an unusual direction. The consideration of such tradeoffs are why asserted motivations or suggestions to combine or modify references must be supported by objective evidence and broad conclusory statements are not evidence. *In re Lee*, 277 F.3d at 1343, 61 U.S.P.Q.2d at 1433-34; *In re Kotzab*, 217 F.3d at 1370, 55 U.S.P.Q.2d at 1317; *In re Dembiczak*, 175 F.3d at 999, 50 U.S.P.Q.2d at 1616-17.

The foregoing notwithstanding, the proposed modification to incorporate one-bit counters for the two-bit counters as taught in both *Patt* and *Talcott* changes the principle of operation of the references, for the reasons discussed hereinabove. Consequently, there can be no suggestion or motivation to modify the references to make the claimed invention. MPEP § 2143.01.

For at least the reasons discussed above, the Applicant respectfully asserts that claim 10 is not *prima facie* obvious in view of *Patt*, *Talcott* and *Shimomura*. Therefore claim 10 is allowable under 35 U.S.C. § 103 over *Patt*, *Talcott* and *Shimomura*.

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2 *Talcott* explicitly discloses the use of two-bit counters. *Talcott*, column 3, line 66.

Claim 30 depends from claim 28 and is directed to the processing system thereof in which each entry in the tables comprises a 1-bit counter. Claim 28, discussed further below, has been rejected as being unpatentable over *Patt* and *Talcott*. (Paper No. 11, page 8.) The Examiner rejects claim 30 on the same basis as claim 10. (Paper No. 11, page 4.) For the same reasons that claim 10 is allowable under 35 U.S.C. § 103, the Applicant respectfully asserts that claim 30 is also allowable.

II. REJECTION UNDER 35 U.S.C. § 103

Claims 21-29 and 31-40 have been rejected under 35 U.S.C. § 103 as being unpatentable over *Patt* in view of *Talcott*. The Applicant respectfully traverses the rejection of claims 21-29 and 31-40 under 35 U.S.C. § 103.

Claim 21 is directed to branch prediction circuitry. As rewritten hereinabove to more particularly point out that which the Applicant regards as the invention, the circuitry includes a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address, a fetch-based branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of the branch address and bits from a history register, each entry of the fetch-based branch history table operable for containing bits representing a prediction value for a plurality of branches in a fetch group wherein each fetch group is represented by a bit in the history register, and a selector table comprising a plurality of entries each for storing a plurality of selection bits and accessed by a pointer generated from selected bits from the branch address and bits from the history register, each the selector bit used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from the fetch-based history table. (The support for the added element is found, for example, in the Detailed Description, page 28, lines 15-20. The Applicant respectfully submits that no new matter is added thereby.) *Patt* allegedly teaches all of the limitations of claim 21 but for the fetch-based history table. (Paper No. 11, page 5.) The Examiner relies on *Talcott* as teaching the fetch-based branch history accessed table entries. (*Id.*)

As in the rejection of claim 10, to cure the admitted defect in *Patt*, the Examiner engrafts the branch predictor of *Talcott* into *Patt*. (Paper No. 11, page 6.) The Examiner asserts that it would be obvious to implement the branch prediction scheme of *Patt* using the fetch bundle prediction of *Talcott* "to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs." (Paper No. 11, page 6.) There is no evidence that the Examiner has found this motivation in one of the possible sources thereof.[3] *See* MPEP § 2143.01. This is just the type of broad conclusory assertion regarding the teachings of the references that has been deemed to fail to provide a motivation or suggestion for combining references necessary for a *prima facie* showing of obviousness. *In re Lee*, 277 F.3d at 1343, 61 U.S.P.Q.2d at 1433-34; *In re Kotzab*, 217 F.3d at 1370, 55 U.S.P.Q.2d at 1317; *In re Dembiczak*, 175 F.3d at 999, 50 U.S.P.Q.2d at 1616-17. As previously noted such motivations cannot be sufficient as they render the requirement nugatory. Furthermore, to the extent the Examiner is relying on objective evidence at all, it is evidence gleaned solely from the Application. (*See e.g.* Background Information, page 3, lines 7-10.) A showing of obviousness cannot be predicated on knowledge gleaned only from the Application. *In re McLaughlin*, 443 F.2d at 1395, 170 U.S.P.Q. at 212.

Neither has the Examiner provided any evidence of a reasonable expectation of success in modifying *Patt* to make the claimed invention. Such a showing is also required to make a *prima facie* showing of obviousness. MPEP § 2143. The reasonable expectation of success must be found in the prior art, not the Application. *Id.* The Examiner is using the Application as a template to reconstruct the invention from parts harvested from the references, and thus, any expectation of success is derived solely from the Application.

Moreover, *Talcott* teaches the use of a gshare predictor in the mechanism described therein. (*Talcott*, column 4, lines 21-22.) The gshare predictor described by *McFarling*, "Combining Branch Predictors" discussed hereinbelow, does not disclose fetch-based accessing. (*See McFarling*, page 6, § 5; pages 11-12, § 7.) In particular, the history register of *McFarling*

3 The Examiner cites to *Talcott* at column 1, lines 54-67. This teaching does not stand for the stated proposition. *Talcott* is generally discussing branch prediction and the increased chance of multiple branch instructions being processed in a single fetch cycle as the number of pipelines increases.

records the direction of the most recent *n* conditional branches, without any reference to a "fetch group." (*McFarling*, page 6, § 5.) Consequently, neither *Patt* nor *Talcott* teach or suggest all of the limitations of claim 21.

For at least the reasons discussed above, the Applicant respectfully asserts that claim 21 is not *prima facie* obvious in view of *Patt* and *Talcott*. Therefore claim 21 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*

Claim 22 is directed to the branch prediction circuitry of Claim 21 and further comprising circuitry for updating the bimodal and fetch-based branch history tables operable to set a corresponding entry in each of the bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time, and set a corresponding entry in each of the bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time. The Examiner admits that neither *Patt* nor *Talcott*, alone or in combination, teach or suggest the limitations of claim 22. (Paper No. 11, page 6.) Nevertheless, the Examiner contends that *Patt* teaches that it was known to use the most accurate branch prediction. (Paper No. 11, page 6) (citing *Patt*, §§ 4, 4.1 ¶¶ 1-3). The Examiner is referring to teaching in *Patt* that discloses that the BPST keeps track of the more accurate predictor for branches at different branch execution states, and the counter associated with a hash into the BPST is used to select the appropriate prediction. (*Patt*, §§ 4, 4.1 ¶¶ 1-3.) From this, the Examiner concludes that it "would have been obvious to one of ordinary skill in the art at the time of the invention to implement *Patt* and Talcott's hybrid branch prediction as updating entries in each of the bimodal and fetch-based tables with one or the other value based upon the accuracy of prediction based on *Patt's* teaching." (Paper No. 11, pages 6-7.)

As an initial matter, there is no "*Patt* and *Talcott's*" hybrid branch predictor. *Patt* teaches hybrid predictors. (*Patt*, § 2.) *Talcott* teaches a mechanism for performing multiple branch predictions per cycle. (*Talcott*, column 1, lines 7-9.) "*Patt* and *Talcott's*" hybrid predictor is a fictional device that results from the incorporation of *Talcott's* teaching into that of *Patt* to recreate the invention of claim 21 from which claim 22 depends, with no suggestion to do so but for the Application itself.

That engrafting having been accomplished, the Examiner then proceeds to make the aforementioned allegation as to obviousness. However, the Applicant notes that the Examiner's reference to "*Patt's* suggestion" leaves the impression that *Patt* suggests updating as recited in claim 22. The suggestion is rather an inference drawn by the Examiner from the teaching in *Patt* mentioned hereinabove with respect to the BPST keeping track of the more accurate predictor again with the inferences guided with the aid of the Applicant's disclosure. The Examiner provides no objective evidence to support that assertion that this teaching in *Patt* suggests the limitation of claim 22.

For at least the reasons discussed above, the Applicant respectfully asserts that claim 22 is not *prima facie* obvious in view of *Patt* and *Talcott*. Therefore claim 22 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 24 is directed to the branch prediction circuitry of Claim 21 and further comprising circuitry for updating the selector table operable to update a corresponding bit in a selected entry in the selector table with a first value when a bimodal prediction value from the bimodal branch history table correctly represents a corresponding branch resolution, and update a corresponding bit in a selected entry in the selector table with a second value when a fetch-based prediction value from the fetch-based branch history table correctly represents the corresponding branch resolution. Claim 24 incorporates the limitations of claim 21 from which it depends, and is therefore necessarily allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 25 is directed to the branch prediction circuitry of Claim 21 wherein the plurality of selection bits are operable for selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table. The Examiner asserts that this is taught by the combination of *Patt* and *Talcott* because *Patt* teaches that "the selector selects one branch predictor when it is useful and the other when it is useful." (Paper No. 11, page 7.) The Examiner's assertion fails for several reasons. Plainly it does not address the limitation of claim 25. Claim 25 does not recited selecting one branch predictor when it is useful and the other when it is useful. Furthermore, it is indisputable that neither *Patt* nor *Talcott*, alone or in combination teach or suggest the limitation of claim 25. *Patt*

does not teach the prediction of branches in a fetch group and cannot, therefore, teach selecting a first subset of prediction values... and a second subset of prediction values... because there are no first and second subset of prediction values at all. Conversely, *Talcott* does not teach combined branch predictors and therefore necessarily fails to teach or suggest the first and second subsets of prediction values as recited in claim 25 because there is no bimodal branch history table and fetch-based branch history table from which subsets of predictions are made. Thus, neither *Patt* nor *Talcott* teach or suggest the limitation of claim 25. The Examiner has provided no motivation or suggestion for combining the references beyond that recited with respect to claim 21.

For at least the reasons discussed above, the Applicant respectfully asserts that claim 25 is not *prima facie* obvious in view of *Patt* and *Talcott*. Therefore claim 25 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 28 recites a processing system including a first branch history table comprising a plurality of bimodally accessed entries, each entry for storing a first set of branch prediction bits, a second branch history table comprising a plurality of fetch-based accessed entries each entry for storing a second set of branch prediction bits, a selector for selecting, in response to a plurality of selection control bits, a set of prediction bits from a selected one of the sets of bits accessed from the first and second branch history tables, and a selector table comprising a plurality of entries, each entry for storing a plurality of selection control bits wherein the selection control bits are set as a function of a performance history of corresponding first and second sets of branch prediction bits stored in the first and second branch history tables. Claim 28 has been rejected on the same basis as claim 21. (*Cf.* Paper No. 11, pages 5-6, 8-9.) For at least those reasons discussed in conjunction with claim 21 hereinabove, the Applicant also respectfully asserts that claim 28 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 29 is directed to the processing system of Claim 28 wherein the entries of the selector table are accessed using fetch-based accessing. Claim 29 has been rejected on teaching in *Talcott* directed to a mechanism for predicting multiple branches in a fetch bundle. (Paper No. 11, page 9) (citing *Talcott*, column 3, line 58 through column 4, line 25). The Examiner asserts

that that it would be obvious to implement the branch prediction scheme of *Patt* using the fetch bundle prediction of *Talcott* "to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs." (Paper No. 11, page 9.) The Examiner provided the same motivation with respect to, *inter alia*, claim 10, and it is equally unavailing with respect to claim 29.

The Examiner also states that the two-level single predictor and the two-level hybrid predictor mechanism function much the same, leading one to adapt what is adapted for one to the other, namely, fetch-based accessing. (Paper No. 11, page 9.) These allegations fail for several reasons. There is no evidence offered to support the assertion that a two-level single predictor and two-level hybrid predictor function much the same. Indeed, the Examiner provides no explanation what is meant by much the same functioning. There is no objective evidence to normalize the assertion; it could mean anything. The factual question of motivation is material to patentability and cannot be resolved on subjective belief and unknown authority. *In re Lee*, 277 F.3d at 1343-44, 61 U.S.P.Q.2d at 1434.

Moreover, a *prima facie* showing of obviousness also requires that there be a reasonable expectation of success in combining the references to make the claimed invention. MPEP § 2143. This expectation of success must be found in the prior art, not the Applicant's disclosure. *Id.* No such evidence has been presented.

For at least the reasons discussed above, the Applicant respectfully asserts that claim 29 is not *prima facie* obvious in view of *Patt* and *Talcott*. Therefore claim 29 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

With respect to claim 31 directed to the processing system of Claim 28 in which the first and second branch history tables and the selector table form a portion of a branch execution unit "BXU." Because claim 32 incorporates the limitations of claim 28, it is also allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*. Similarly, claim 32 directed to the system of claim 31 in which the BXU forms part of a microprocessor, and claim 32 directed to the system of claim 33 and further including memory coupled to the microprocessor are also allowable under 35 U.S.C. § 103.

Claim 34 is directed to a method of performing branch predictions in a processing system including a bimodal branch history table, a fetch-based branch history table and a selector table. The method comprises accessing the bimodal branch history table to retrieve a first set of branch prediction bits, accessing the fetch-based branch history table to retrieve a set of second branch prediction bits, selecting between the first and second sets of branch prediction bits in response to corresponding bits retrieved from the selector table, wherein a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits is not less than a number of instructions in a fetch group, and updating the selector table as a function of actual branch resolution. The Examiner admits that *Patt* does not teach a fetch-based branch history table as recited in claim 34. (Paper No. 11, page 11.) The Examiner seeks to cure the admitted deficiency in *Patt* by relying on *Talcott* as teaching a mechanism to provide multiple branch predictions for branches within a fetch bundle. (Paper No. 11, page 11) (citing *Talcott*, column 3, line 58 through column 4, line 25). The Examiner's motivation for combining the references to incorporate the mechanism of *Talcott* into *Patt* is to increase branch prediction accuracy for many branches. (Paper No. 11, pages 11-12.) However, this is unavailing. This may have been *Talcott's* motivation for the branch prediction mechanism disclosed therein but does not provide any rationale for combining *Talcott* and *Patt*. Moreover, such broad conclusory statements are not evidence. *In re Lee*, 277 F.3d at 1343, 61 U.S.P.Q.2d at 1433-34; *In re Kotzab*, 217 F.3d at 1370, 55 U.S.P.Q.2d at 1317; *In re Dembiczak*, 175 F.3d at 999, 50 U.S.P.Q.2d at 1616-17.

With respect to the recitation in claim 34 directed to a sum of a number of bits in the first and second branch predictions is not less than a number of instructions in a fetch group, the Examiner admits that neither *Patt* nor *Talcott* teach or suggest these limitations. (Paper No. 11, page 12.) Moreover, *Talcott* explicitly teaches a mechanism where the number of prediction counter values is less than the number of instructions in a fetch bundle. (*Talcott*, column 3, lines 67-68.) Furthermore the references would not be expected to teach such a limitation because *Patt* did not consider the prediction of multiple branches, and *Talcott* does not consider combined predictors. Nevertheless, the Examiner, undaunted by the lack of teaching and having engrafted the predictor of *Talcott* into the hybrid predictor of *Patt*, now concludes that it would

have been obvious that "if one bit came from the first table and one bit came from the second table it would be not less than the instructions in a fetch group if that group were composed of two instructions." (Paper No. 11, page 12.) While the Applicant cannot dispute the conclusion of the triple hypothetical as it only states that one plus one is two, there is no teaching in either of the references, nor is there a recitation in the claim to which it pertains. There is no teaching in either of the references that suggests a first bit coming from a first table and a second bit coming from a second table. The Examiner is relying solely on knowledge gleaned from the Applicant's disclosure. As to the motivation for two instructions in a fetch group, the Examiner contends that it is to reduce instruction throughput. (Paper No. 11, page 12.) Apparently having improved the performance *Patt* too much by incorporating *Talcott*, this in one of those rare circumstances where one of ordinary skill in the art would be motivated to reduce the performance of the reference. Plainly, such motivations as asserted by the Examiner exemplify the requirement that a motivation or suggestion to combine references must be grounded in objective evidence that is clear and particular. For at least the reason that the references, alone or in combination, do not teach or suggest all of the limitations of claim 34, and because there is no motivation from one of the possible sources thereof, a *prima facie* showing of obviousness has not been made with respect to claim 34. Therefore claim 34 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 35 is directed to the method of Claim 34 wherein the step of updating the selector table comprises the substeps of determining if at least one of the first set of branch prediction bits correctly predicts the corresponding branch resolution outcome, updating the corresponding entry in the selector table to a first logic value when the at least one of the first set of prediction bits correctly represents the branch resolution outcome, determining if at least one of the second set of branch prediction bits correctly predicts the branch resolution outcome, and updating the corresponding entry in the selector table to a second logic value when the at least one of the second set of branch prediction bits correctly represents the branch resolution outcome. *Patt* allegedly teaches the limitations of claim 35 is discussing hybrid branch predictors. (Paper No. 11, page 13) (citing *Patt*, § 2). However, *Patt* does not disclose first and second set of branch prediction bits, and thus, necessarily does not and cannot disclose updating... when the at least

one of the first set of prediction bits correctly... , and updating... when the at least one of the second set of prediction bits correctly... . Because the *Patt* and *Talcott*, alone or in combination, do not teach or suggest all of the limitations of claim 35, and because there is no motivation to combine the references to make the claimed invention, claim 35 is not *prima facie* obvious. Therefore claim 35 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 36 is directed to the method of Claim 35 and further comprising the steps of determining if at least one bit of both the first and second sets of branch history bits correctly predict the branch resolution outcome, maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome, determining if at least one bit of both the first and second sets of branch prediction bits incorrectly predict the branch resolution outcome, and maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch history bits incorrectly predict the branch history outcome. Claim 36 has been rejected on the same teaching in *Patt* as relied upon in rejecting claim 35. (Paper No. 11, pages 13-14.) However, *Patt* does not disclose first and second set of branch prediction bits, and thus, necessarily does not and cannot disclose maintaining... when the at least one of the first set of prediction bits incorrectly predicts... , and maintaining... when the at least one of the second set of prediction bits incorrectly predicts... . Because the *Patt* and *Talcott*, alone or in combination, do not teach or suggest all of the limitations of claim 36, and because there is no motivation to combine the references to make the claimed invention, claim 36 is not *prima facie* obvious. Therefore claim 36 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 37 is directed to the method of Claim 35 and further comprising the steps of determining whether at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome, maintaining the current value of corresponding bits in the corresponding selector table entry when at the least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome, and updating the current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly

predicts the branch resolution outcome. Claim 37 has been rejected on the same teaching in *Patt* as relied upon in rejecting claim 35. (Paper No. 11, pages 13-14.) However, *Patt* does not disclose first and second set of branch prediction bits, and thus, necessarily does not and cannot disclose maintaining... when the at least one of the first set of prediction bits incorrectly predicts... , and maintaining... when the at least one of the second set of prediction bits incorrectly predicts... . The Examiner admits that neither *Patt* nor *Talcott* teach or suggest the limitation of updating a current selector table to a logic value associated with the fetch-based branch history table. (Paper No. 11, page 14.) Nonetheless, the Examiner states that *Patt* demonstrated that two-level branch predictors is the highest performance of the single predictors. (Paper No. 11, page 14.) However, the teaching in *Patt* is that gshare is a variation of the highest performing single-scheme predictor, namely the Two-Level Adaptive Branch Predictor. (*Patt*, page 235, § 3.1, ¶ 2.) Thus gshare is not the Two Level Adaptive Predictor. Moreover, the Examiner's motivation is that this would gradually move the predictor to the more likely correct future choice. (Paper No. 11, page 15.) However, *Patt*, describing the teaching of *McFarling* with respect to hybrid branch predictors expressly discloses that in the mechanism of *McFarling*, the selectors are left unchanged if both predictors are incorrect. (*Patt*, page 252. § 2.) (The Applicant notes that the Examiner relies on this teaching in rejecting claim 26. *See* Paper No. 11, page 16.) Because the *Patt* and *Talcott*, alone or in combination, do not teach or suggest all of the limitations of claim 37, and because there is no motivation to combine the references to make the claimed invention, claim 37 is not *prima facie* obvious. Therefore claim 37 is allowable under 35 U.S.C. § 103 over *Patt* and *Talcott*.

Claim 38 is directed to the method of Claim 34 wherein said step of accessing the fetch-based branch history table comprises the substep of generating an address from at least some bits of a branching instruction and bits retrieved from a history register. Claim 39 is directed to the method of Claim 38 wherein the history register comprises a shift register. Each of these claims incorporate the limitations of their base claim. Therefore, claims 38 and 39 are necessarily allowable under 35 U.S.C. § 103 over *Patt* and *Talcott* as well.

III. REJECTION UNDER 35 U.S.C § 103

Claims 23, 26, 27 and 40 have been rejected 35 U.S.C § 103 over *Patt* in view of *Talcott* in further view of *McFarling*, "Combining Branch Predictors." The Applicant respectfully traverses the rejection of claims 23, 26, 27 and 40 under 35 U.S.C. § 103.

Claim 23 is directed to the branch prediction circuitry of Claim 21 wherein the history register comprises a shift register and the branch prediction circuitry further comprises circuitry for updating the shift register by shifting in a preselected prediction value for each fetch group. The Examiner admits that neither *Patt* nor *Talcott* teach or suggest the limitations of claim 23. (Paper No. 11, page 16.) The Examiner relies on *McFarling* as teaching a history register using a shift register. (Paper No. 11, page 16.) However, *McFarling* does not teach shifting in a preselected prediction value for each fetch group. There is no concept of a fetch group in *McFarling*. The Examiner asserts that it would have been obvious to implement the fetch groups of *Patt* and *Talcott* with a shift register of *McFarling* in order to use existing technology. (Paper No. 11, page 16.) Again, such broad conclusory statements are not evidence. *In re Lee*, 277 F.3d at 1343, 61 U.S.P.Q.2d at 1433-34; *In re Kotzab*, 217 F.3d at 1370, 55 U.S.P.Q.2d at 1317; *In re Dembiczak*, 175 F.3d at 999, 50 U.S.P.Q.2d at 1616-17. Moreover as the Applicant has previously discussed, there is no motivation for engrafting the mechanism of *Talcott* into *Patt* as previously discussed hereinabove. The foregoing notwithstanding, even after all of the reconstruction, the result does not yield the invention of claim 23 because, still, there is no updating by shifting in a preselected prediction value for each fetch group. On the contrary, *Talcott* expressly discloses the use of a gshare mechanism. (*Talcott*, column 4, lines 20-23.) The teaching in *McFarling* upon which the Examiner relies with respect to the shift register plainly discloses that the gshare mechanism uses a global history vector recording the direction taken by the most recent *n* branches. Again, there is no concept of a fetch group, and in particular, shifting in a preselected prediction value for each fetch group. Neither *Talcott*, *Patt* nor *McFarling*, alone or in combination teach or suggest all of the limitations of claim 23. No motivation or suggestion for combining or modifying the references to make the claimed invention from one of the possible sources thereof has been provided. Consequently, claim 23 is

not *prima facie* obvious over *Talcott*, *Patt* and *McFarling*. Therefore, claim 23 is allowable under 35 U.S.C. § 103.

Claim 26 is directed to the branch prediction circuitry of Claim 23 wherein the circuitry for updating the selector table is further operable to maintain a value in a selected entry in the selector table when corresponding values from the bimodal and fetch-based branch history tables both correctly represent a corresponding branch resolution, and wherein the circuitry for updating the selector table is further operable to maintain a value in a selected entry in the selector table when neither values from the bimodal and fetch-based branch history tables correctly represent a corresponding branch resolution. Claim 26 incorporates the limitations of claim 23 from which it depends. Because, for the reasons discussed hereinabove claim 23 is allowable under 35 U.S.C. § 103, claim 26 is also necessarily allowable.

Claim 27 is directed to the branch prediction circuitry of Claim 23 wherein the circuitry for updating the selector table is further operable to set a value in a selected entry in the selector table to a value associated with the fetch-based table when corresponding values from the bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome. Claim 27 has been rejected on the same basis as claim 37, discussed hereinabove. (*Cf.* Paper No. 11, pages 14-15; page 17.) Again, the Examiner's motivation for modifying or combining the references fails is inconsistent with the express teaching of *Patt* as it related to the hybrid predictors of *McFarling*. Consequently, the references alone or in combination do not teach or suggest the limitations of claim 27, nor is there a motivation or suggestion to combine or modify the references to make the invention of claim 27. Thus, claim 23 is not *prima facie* obvious over *Talcott*, *Patt* and *McFarling* and claim 27 is allowable under 35 U.S.C. § 103.

Claim 40 is directed to the method of Claim 39 wherein the method further comprises the steps of updating the shift register by shifting in a prediction bit for each fetch group. Claim 40 has been rejected on the same basis as claim 23, discussed above. (*Cf.* Paper No. 11, page 15-16 and 16-17.) For at least the reasons discussed in conjunction with claim 23, the references, alone or in combination do not teach or suggest the limitations of claim 40, nor is there a motivation to

combine or modify the references to make the invention of claim 40. Thus, claim 40 is not *prima facie* obvious over *Talcott*, *Patt* and *McFarling* and claim 40 is allowable 35 U.S.C. § 103.

IV. CONCLUSION

As a result of the foregoing, it is asserted by the Applicants that the remaining claims in the Application are in condition for allowance, and respectfully request an early allowance of such claims.

Applicant respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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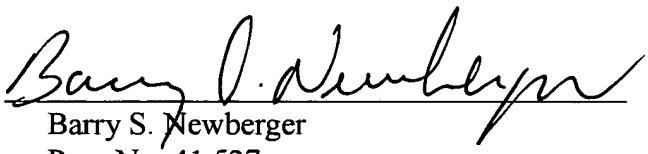
By: 
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